TWO CHANNEL, CURRENT-LIMITED, POWER-DISTRIBUTION SWITCHES

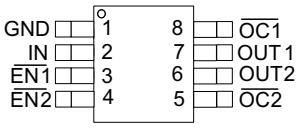
FEATURES

- **70-mΩ High-Side MOSFET**
- **1-A Continuous Current**
- **Thermal and Short-Circuit Protection**
- **Accurate Current-Limit (1.2 A min, 2 A max)**
- **Operating Range: 2.7 V to 5.5 V**
- **0.6-ms Typical Rise Time**
- **Undervoltage Lockout**
- **Deglitched Fault Report ($\overline{OCx}$)**
- **No $\overline{OCx}$ Glitch During Power Up**
- **1-μA Maximum Standby Supply Current**
- **Bidirectional Switch**
- **Ambient Temperature Range: –40°C to 85°C**
- **Built-in Soft-Start**
- **UL Listed -- File No. E169910, Both Single and Ganged Channel Configuration**

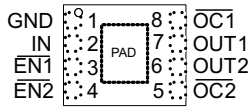
APPLICATIONS

- **Heavy Capacitive Loads**
- **Short-Circuit Protection**

TPS2062A/TPS2066A
D PACKAGE
(TOP VIEW)



TPS2062A/TPS2066A
DRB PACKAGE
(TOP VIEW)



Enable inputs are active low for all TPS2062A and active high for all TPS2066A

DESCRIPTION

The TPS206xA power-distribution switches are intended for applications where heavy capacitive loads and short-circuits are likely to be encountered. The TPS206xA family is pin-for-pin compatible with the TPS206x family with a tighter overcurrent tolerance. This family of devices incorporates two 70-mΩ N-channel MOSFET power switches for power-distribution systems that require multiple power switches in a single package. Each switch is controlled by a logic enable input. Gate drive is provided by an internal charge pump designed to control the power-switch rise and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

Each device limits the output current to a safe level by switching into a constant-current mode when the output load exceeds the current-limit threshold or a short is present. Individual channels indicate the presence of an overcurrent condition by asserting its corresponding $\overline{OCx}$ output (active low). Thermal protection circuitry disables the device during overcurrent or short-circuit events to prevent permanent damage. The device recovers from thermal shutdown automatically once the device has cooled sufficiently. The device provides undervoltage lockout to disable the device until the input voltage rises above 2.0 V. The TPS206xA is designed to current limit at 1.6 A typically per channel.

GENERAL SWITCH CATALOG

33 mΩ, single	80 mΩ, single	80 mΩ, dual	80 mΩ, dual	80 mΩ, triple	80 mΩ, quad	80 mΩ, quad
TPS201xA 0.2 A - 2 A	TPS2014 600 mA	TPS2042B 500 mA	TPS2080 500 mA	TPS2043B 500 mA	TPS2044B 500 mA	TPS2085 500 mA
TPS202x 0.2 A - 2 A	TPS2015 1 A	TPS2052B 500 mA	TPS2081 500 mA	TPS2053B 500 mA	TPS2054B 500 mA	TPS2086 500 mA
TPS203x 0.2 A - 2 A	TPS2041B 500 mA	TPS2046B 250 mA	TPS2082 500 mA	TPS2047B 250 mA	TPS2048A 250 mA	TPS2087 500 mA
	TPS2051B 500 mA	TPS2056 250 mA	TPS2090 250 mA	TPS2057A 250 mA	TPS2058 250 mA	TPS2095 250 mA
	TPS2045A 250 mA	TPS2062 1 A	TPS2091 250 mA	TPS2063 1 A		TPS2096 250 mA
	TPS2049 100 mA	TPS2066 1 A	TPS2092 250 mA	TPS2067 1 A		TPS2097 250 mA
	TPS2055A 250 mA	TPS2060 1.5 A				
	TPS2061 1 A	TPS2064 1.5 A				
	TPS2065 1 A					
	TPS2068 1.5 A					
	TPS2069 1.5 A					

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PowerPAD is a trademark of Texas Instruments.

This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriate logic voltage level, preferably either VCC or ground. Specific guidelines for handling devices of this type are contained in the publication Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies available from Texas Instruments.

AVAILABLE OPTION AND ORDERING INFORMATION

T_A	ENABLE	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT	TYPICAL SHORT-CIRCUIT LIMIT	PACKAGE(1)			
				D-8 (SOIC)		DRB-8 (SON)	
				PART #	STATUS	PART #	STATUS
–40°C to 85°C	Active low	1 A	1.6 A	TPS2062AD	AVAILABLE	TPS2062ADRB	AVAILABLE
	Active high			TPS2066AD	AVAILABLE	TPS2066ADRB	AVAILABLE

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating temperature range unless otherwise noted(1)(2)

			VALUE	UNIT
V_I	Input voltage range	IN	–0.3 to 6	V
V_O	Output voltage range	OUTx	–0.3 to 6	V
V_I	Input voltage range	$\overline{ENx}$, ENx	–0.3 to 6	V
	Voltage range	$\overline{OCx}$	–0.3 to 6	V
I_O	Continuous output current	OUTx	Internally limited	
	Continuous total power dissipation		See "Dissipation Rating Table"	
T_J	Operating junction temperature range		–40 to 125	°C
T_{stg}	Storage temperature range		–65 to 150	°C
ESD	Electrostatic discharge protection	Human body model MIL-STD-883C	2	kV
		Charge device model (CDM)	500	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND.

DISSIPATION RATING TABLE

BOARD	PACKAGE	THERMAL RESISTANCE θ_{JA}	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
Low-K(1)	D-8	170 °C/W	586 mW	5.86 mW/°C	320 mW	234 mW
High-K(2)	D-8	97.5 °C/W	1025 mW	10.26 mW/°C	564 mW	410 mW
Low-K(3)	DRB(4)	270 °C/W	370 mW	3.71 mW/°C	203 mW	148 mW
High-K(5)	DRB(4)	60 °C/W	1600 mW	16.67 mW/°C	916 mW	666 mW

(1) The JEDEC low-K (1s) board used to dervie this data was a 3in x 3in, two-layer board with 2-ounce copper traces on top of the board.
(2) The JEDEC high-K (2s2p) board used to dervive this data was a 3in x 3in, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.
(3) Soldered PowerPAD on a standard 2-layer PCB without vias for thermal pad. See TI application note SLMA002 for further details.
(4) See *Recommended Operating Conditions* Table for PowePad connection guidelines to meet qualifying conditions for CB Certificate
(5) Soldered PowerPAD on a standard 4-layer PCB with vias for thermal pad. See TI application note SLMA002 for further details.

RECOMMENDED OPERATING CONDITIONS(1)

		MIN	MAX	UNIT
V_I	Input voltage, IN	2.7	5.5	V
	Input voltage, $\overline{ENx}$, ENx	0	5.5	V
I_O	Continuous output current, OUTx	0	1	A
T_J	Operating virtual junction temperature	–40	125	°C

(1) The PowePad must be connected externally to GND pin to meet qualifying conditions for CB Certificate (DRB package only)

ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range, V_I = 5.5 V, I_O = 1 A, $V_{/ENx}$ = 0 V (TPS2062A) or V_{ENx} = 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)			MIN	TYP	MAX	UNIT
POWER SWITCH								
$r_{DS(on)}$	Static drain-source on-state resistance	2.7 V ≤ V_I ≤ 5.5 V, I_O = 1 A		T_J = 25°C		70	100	mΩ
				–40°C ≤ T_J ≤ 125°C			135	
t_r	Rise time, output	V_I = 5.5 V	C_L = 1 µF, R_L = 5 Ω, T_J = 25°C			0.6	1.5	ms
		V_I = 2.7 V				0.4	1	
t_f	Fall time, output	V_I = 5.5 V			0.05		0.5	
		V_I = 2.7 V			0.05		0.5	
ENABLE INPUT $\overline{EN}$ OR EN								
V_{IH}	High-level input voltage	2.7 V ≤ V_I ≤ 5.5 V			2			V
V_{IL}	Low-level input voltage						0.8	
I_I	Input current				-0.5		0.5	µA
t_{on}	Turnon time	C_L = 100 µF, R_L = 5 Ω					3	ms
t_{off}	Turnoff time						3	
CURRENT LIMIT								
I_{OS}	Short-circuit output current per channel	V_I = 5 V, OUTx connected to GND, device enabled into short-circuit		T_J = 25°C	1.2	1.6	2.0	A
				–40°C ≤ T_J ≤ 125°C	1.1	1.6	2.1	
I_{OC}	Overcurrent trip threshold	V_{IN} = 5 V			I_{OS}	2.1	2.45	A
I_{OS_G}	Ganged short-circuit output current	V_I = 5 V, OUT1 & OUT2 connected to GND, device enabled into short-circuit		T_J = 25°C	2.4	3.2	4.0	A
				–40°C ≤ T_J ≤ 125°C	2.2	3.2	4.2	
I_{OC_G}	Ganged overcurrent trip threshold	V_I = 5 V, OUT1 & OUT2 tied together			I_{OS_G}	4.2	4.9	
SUPPLY CURRENT								
I_{IL}	Supply current, device disabled	No load on OUT		T_J = 25°C		0.5	1	µA
				–40°C ≤ T_J ≤ 125°C		0.5	5	
I_{IH}	Supply current, device enabled	No load on OUT		T_J = 25°C		50	60	µA
				–40°C ≤ T_J ≤ 125°C		50	75	
I_{lkg}	Leakage current, device disabled	OUT connected to ground		–40°C ≤ T_J ≤ 125°C		1		µA
Reverse leakage current		V_O = 5.5 V, V_I = 0 V		T_J = 25°C		0.2		µA
UNDERVOLTAGE LOCKOUT								
	Low-level input voltage, IN	V_I rising			2		2.5	V
	Hysteresis, IN	V_I falling				75		mV
OVERCURRENT FLAG								
V_{OL}	Output low voltage, $\overline{OC}$	$I_{/OCx}$ = 5 mA					0.4	V
	Off-state current	$V_{/OCx}$ = 5.0 V or 3.3 V					1	µA
	$\overline{OC}$ deglitch	$\overline{OCx}$ assertion or de-assertion			4	8	15	ms
THERMAL SHUTDOWN(2)								
Thermal shutdown threshold					135			°C
Recovery from thermal shutdown					125			°C
Hysteresis						10		°C

(1) Pulsed load testing used to maintain junction temperature close to ambient
(2) The thermal shutdown only reacts under overcurrent conditions.

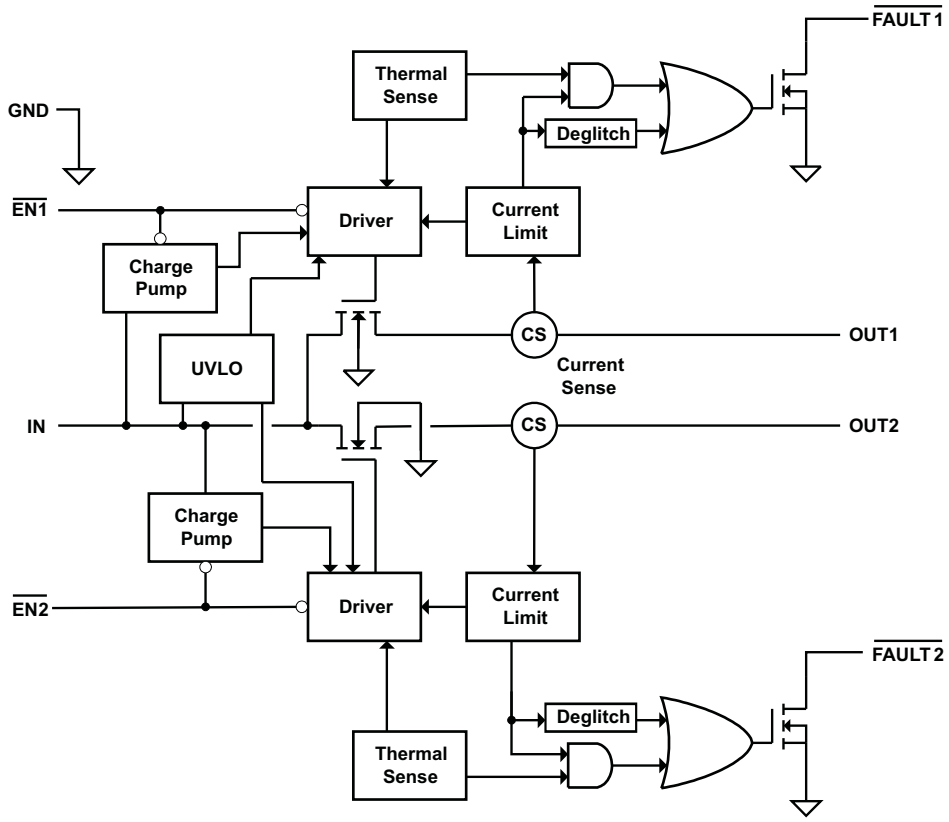
DEVICE INFORMATION

Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	TPS2062A	TPS2066A		
$\overline{EN1}$	3	—	I	Enable input, logic low turns on power switch IN-OUT1
$\overline{EN2}$	4	—	I	Enable input, logic low turns on power switch IN-OUT2
EN1	—	3	I	Enable input, logic high turns on power switch IN-OUT1
EN2	—	4	I	Enable input, logic high turns on power switch IN-OUT2
GND	1	1		Ground
IN	2	2	I	Input voltage
$\overline{OC1}$	8	8	O	Channel 1 over-current indicator; the output is open-drain, active low type
$\overline{OC2}$	5	5	O	Channel 2 over-current indicator; the output is open-drain, active low type
OUT1	7	7	O	Power-switch output, IN-OUT1
OUT2	6	6	O	Power-switch output, IN-OUT2
PowerPAD™ (1)	PAD	PAD		Connect PowerPAD to GND for proper operation (DRB package only)

(1) See the *Recommended Operating Conditions* Table for PowePad connection guidelines to meet qualifying conditions for CB Certificate.

FUNCTIONAL BLOCK DIAGRAM



A. Current sense

B. Active low ($\overline{ENx}$) for TPS2062A. Active high (ENx) for TPS2066A.

PARAMETER MEASUREMENT INFORMATION

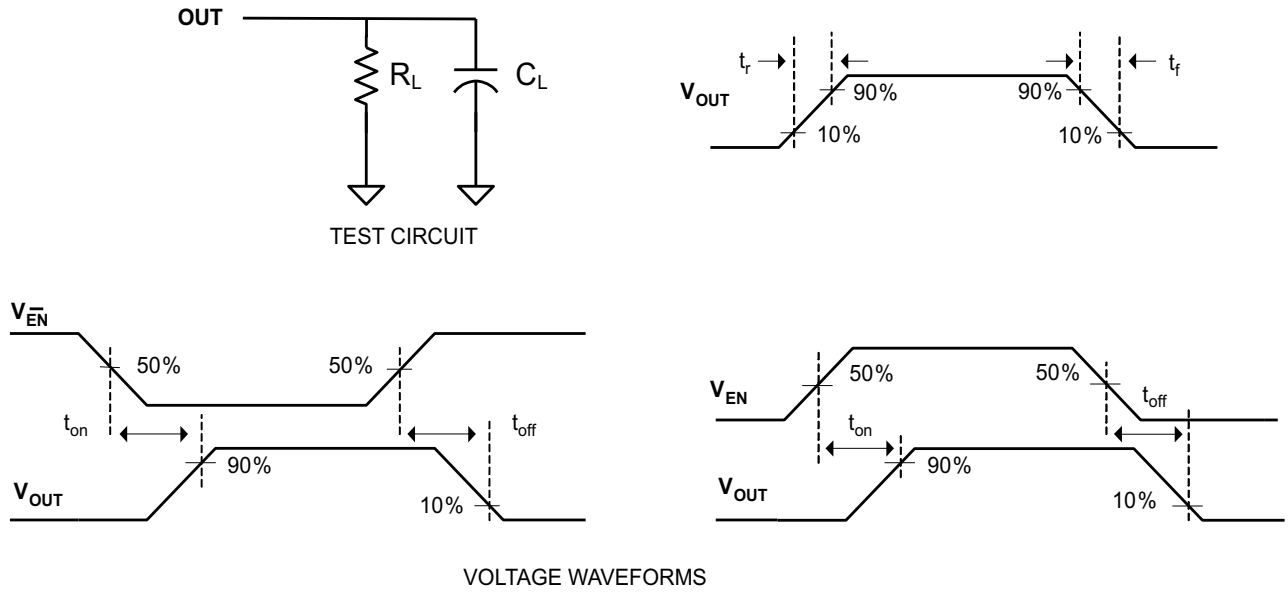


Figure 1. Test Circuit and Voltage Waveforms

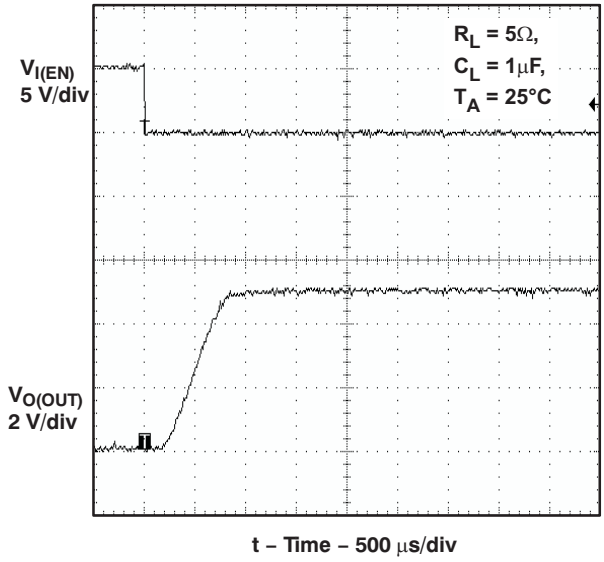


Figure 2. Turnon Delay and Rise Time With 1-μF Load

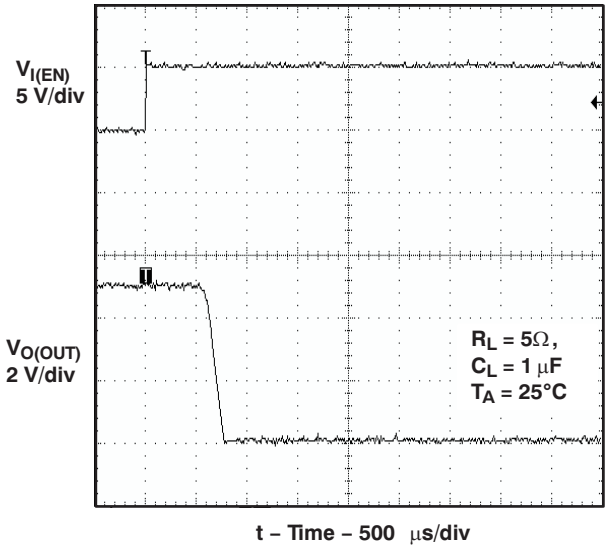


Figure 3. Turnoff Delay and Fall Time With 1-μF Load

PARAMETER MEASUREMENT INFORMATION (continued)

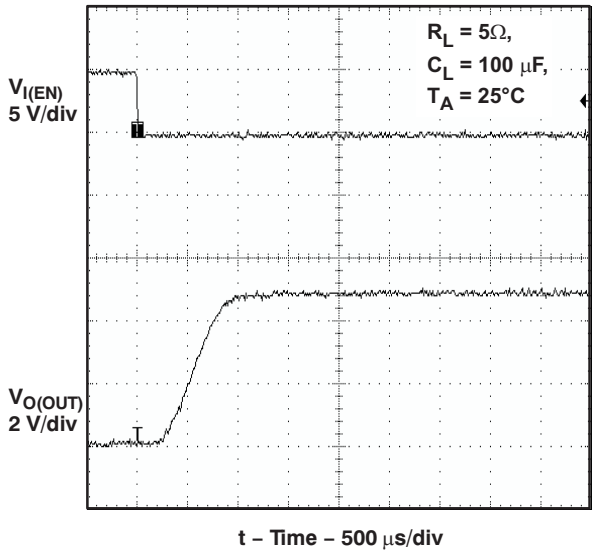


Figure 4. Turnon Delay and Rise Time With 100-μF Load

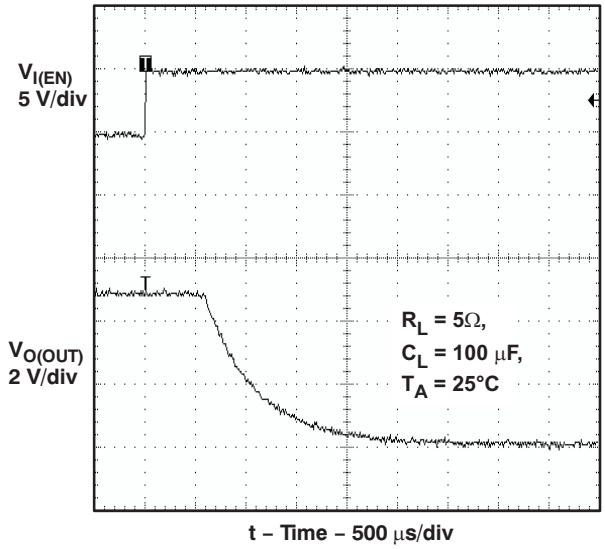


Figure 5. Turnoff Delay and Fall Time With 100-μF Load

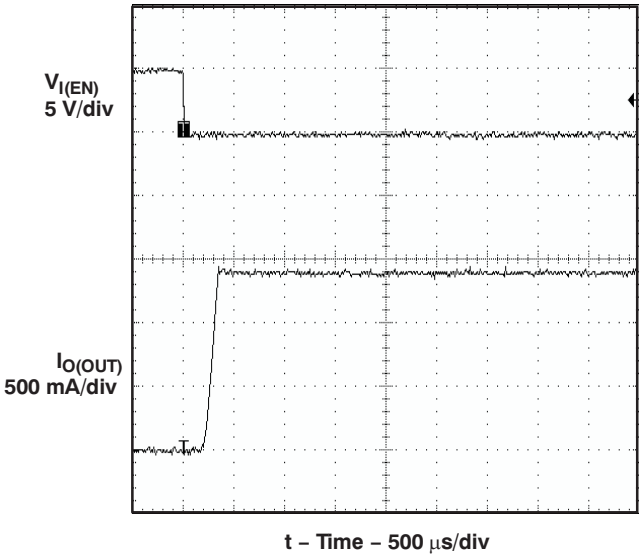


Figure 6. Short-Circuit Current, Device Enabled Into Short

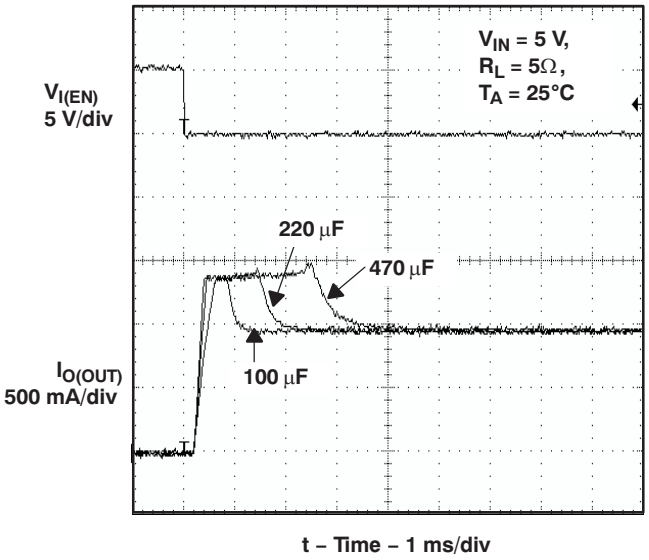


Figure 7. Inrush Current With Different Load Capacitance

PARAMETER MEASUREMENT INFORMATION (continued)

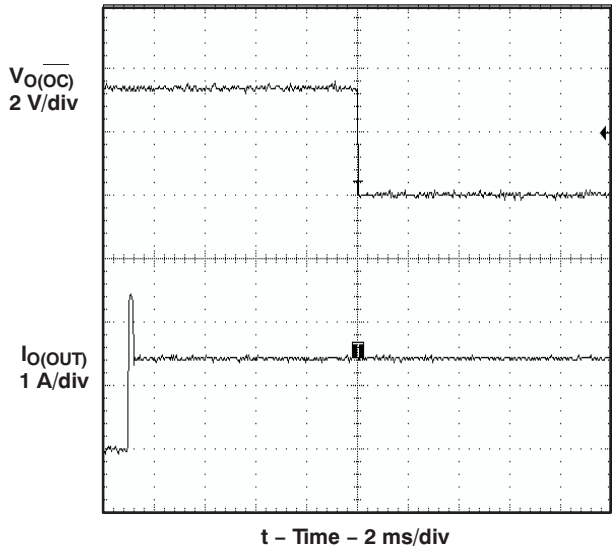


Figure 8. 2-Ω Load Connected to Enabled Device

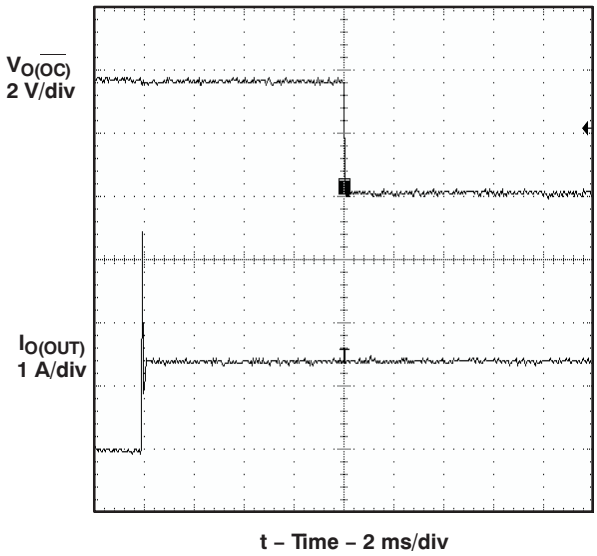


Figure 9. 1-Ω Load Connected to Enabled Device

POWER-SUPPLY CONSIDERATIONS

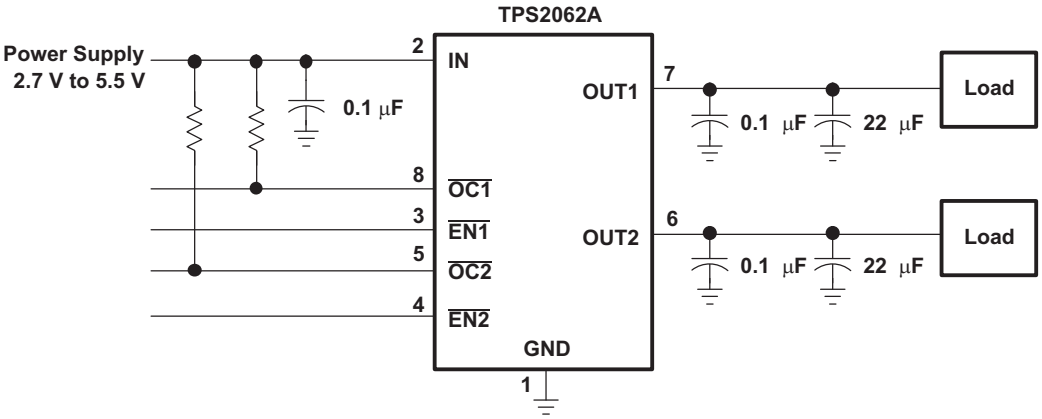


Figure 10. Typical Application

DETAILED DESCRIPTION

OVERVIEW

The devices are current-limited, power distribution switches using N-channel MOSFETs for applications where short-circuits or heavy capacitive loads will be encountered. These devices have a minimum fixed current-limit threshold above 1.1 A allowing for continuous operation up to 1 A per channel. Overtemperature protection is an addtional device shutdown feature. Each device incorporates an internal charge pump and gate drive circuitry necessary to drive the N-channel MOSFETs. The charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires little supply current. The driver controls the gate voltage of the power switch. The driver incorporates circuitry that controls the rise and fall times of the output voltage to provide "soft-start" and to limit large current and voltage surges.

OVERCURRENT

When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Three possible overload conditions can occur.

In the first condition, the output has been shorted before the device is enabled or before voltage is applied to IN. The device senses the short and immediately switches into a constant-current output. In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents may flow for several microseconds before the current-limit circuit can react. The device operates in constant-current mode after the current-limit circuit has responded. In the third condition, the load is increased gradually beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached. The devices are capable of delivering current up to the current-limit threshold without damage. Once the threshold is reached, the device switches into constant-current mode.

Complete shutdown occurs only if the fault is present long enough to activate thermal limiting. The device will remain off until the junction temperature cools approximately 10°C and will then re-start. The device will continue to cycle on/off until the overcurrent condition is removed.

$\overline{\text{OCx}}$ RESPONSE

Each $\overline{\text{OCx}}$ open-drain output is asserted (active low) during an overcurrent or overtemperature condition on that channel. The output remains asserted until the fault condition is removed. The TPS206xA eliminates false $\overline{\text{OCx}}$ reporting by using internal delay circuitry after entering or leaving an overcurrent condition. This "deglitch" time is approximately 8-ms. This ensures that $\overline{\text{OCx}}$ is not accidentally asserted due to normal operation such as starting into a heavy capacitive load. Overtemperature conditions are not deglitched and assert and de-assert the $\overline{\text{OCx}}$ signal immediately.

UNDERVOLTAGE LOCKOUT (UVLO)

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted on/off cycling due to input voltage drop from large current surges.

Enable ($\overline{\text{ENx}}$ or ENx)

The logic enable controls the power switch, bias for the charge pump, driver, and other circuits to reduce the supply current. The supply current is reduced to less than 5 μA when a logic high is present on $\overline{\text{ENx}}$, or when a logic low is present on ENx. A logic low input on $\overline{\text{ENx}}$ or a logic high input on ENx enables the driver, control circuits, and power switch for that channel.

THERMAL SENSE

The TPS206xA monitors the operating temperature of both power distribution switches with individual thermal sensors. The junction temperature of each channel rises during an overcurrent or short-circuit condition. When the die temperature of a particular channel rises above a minimum of 135°C in an overcurrent condition, the internal thermal sense circuitry disables the individual channel in overtemperature to prevent damage. Hysteresis is built into the thermal sensor and re-enables the power switch individually after it has cooled approximately 10°C. The power switch cycles on and off until the fault is removed. This topology allows one channel to continue normal operation even if the other channel is in an overtemperature condition. The open-drain overcurrent flag ($\overline{\text{OCx}}$) is asserted (active low) corresponding to the channel that is in an overtemperature or overcurrent condition.

TYPICAL CHARACTERISTICS

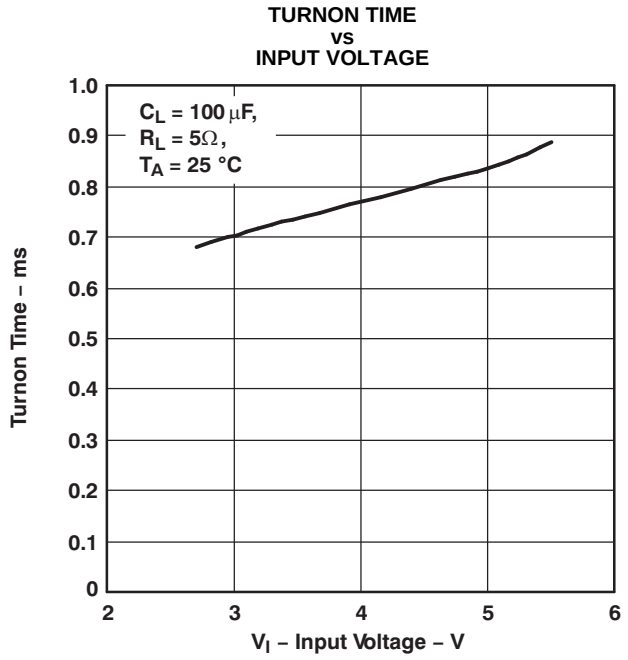


Figure 11.

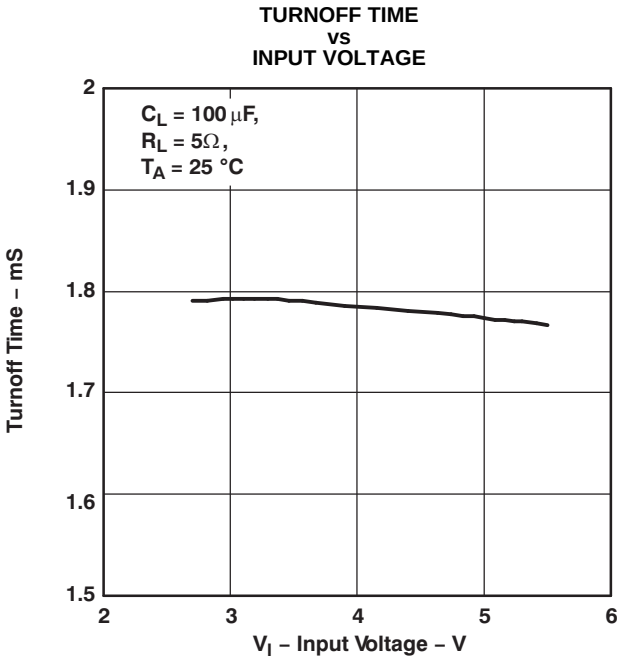


Figure 12.

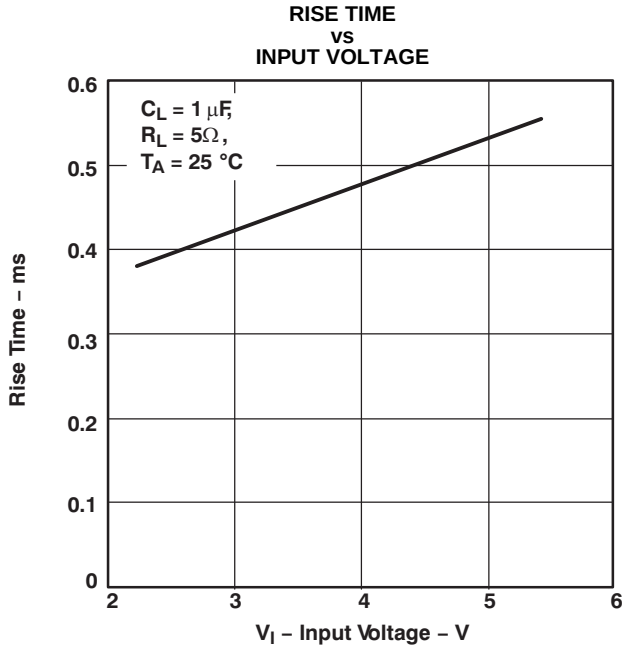


Figure 13.

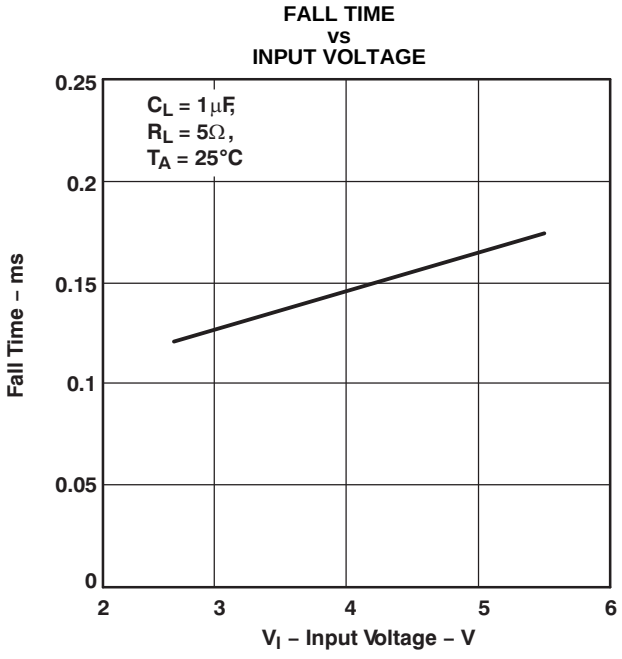


Figure 14.

TYPICAL CHARACTERISTICS (continued)

TPS2062A, TPS2066A
SUPPLY CURRENT, OUTPUT ENABLED
vs
JUNCTION TEMPERATURE

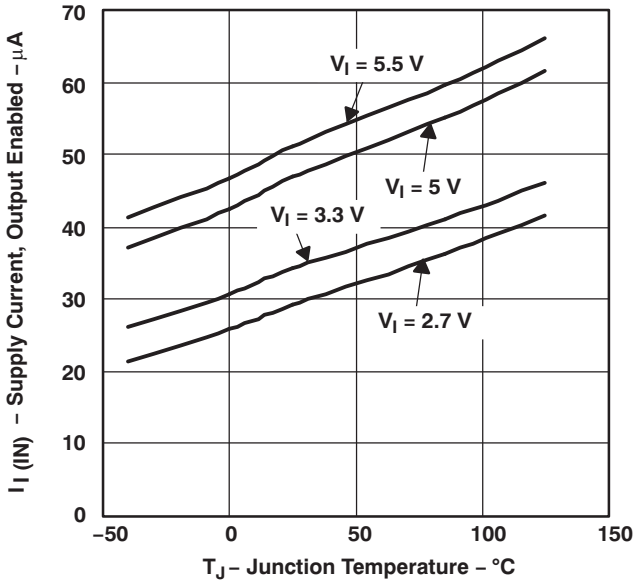


Figure 15.

TPS2062A, TPS2066A
SUPPLY CURRENT, OUTPUT DISABLED
vs
JUNCTION TEMPERATURE

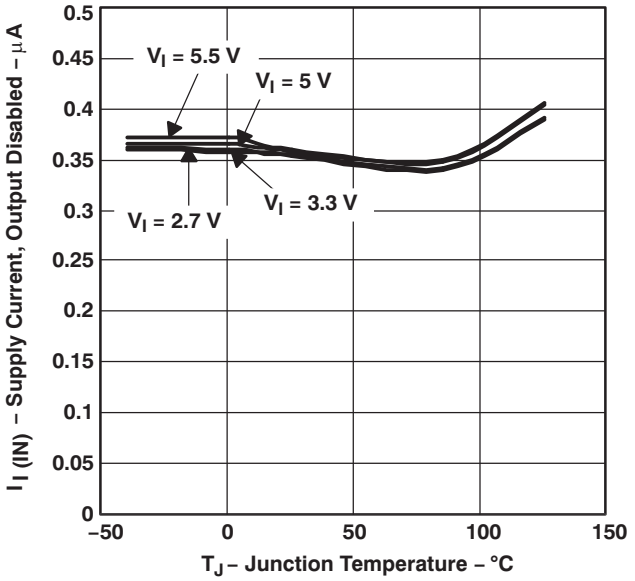


Figure 16.

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

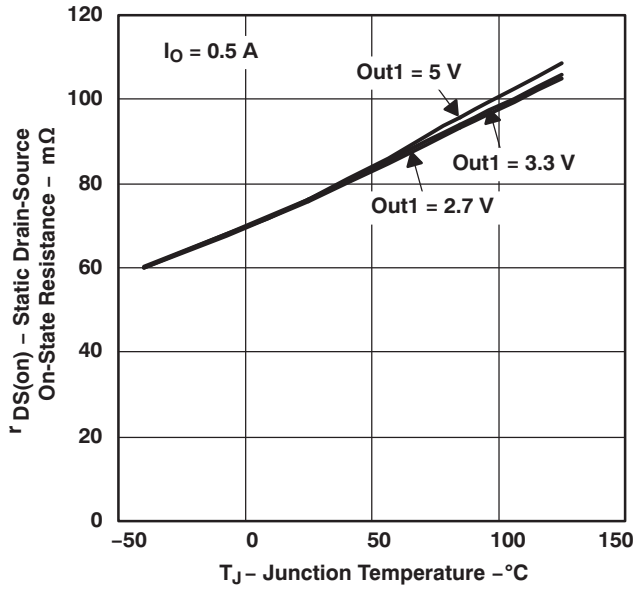


Figure 17.

SHORT-CIRCUIT OUTPUT CURRENT
vs
JUNCTION TEMPERATURE

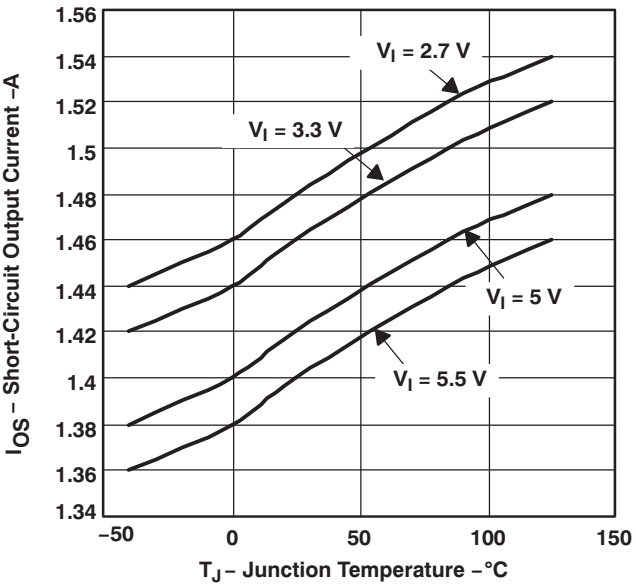


Figure 18.

TYPICAL CHARACTERISTICS (continued)

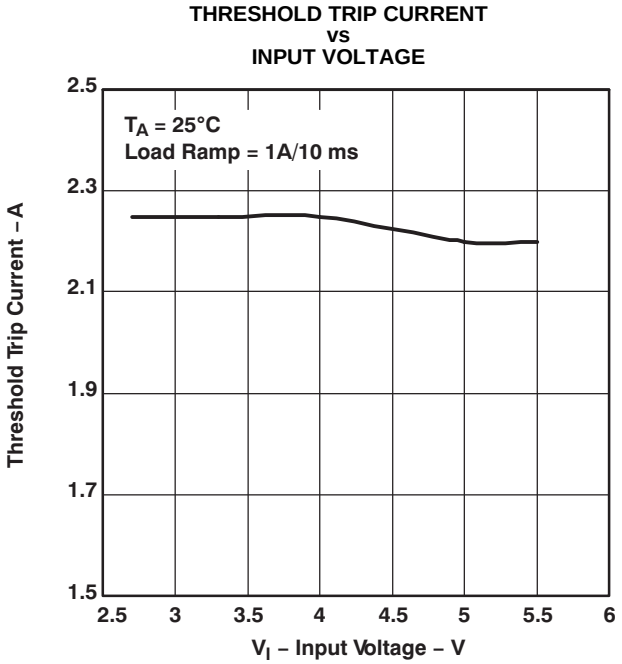


Figure 19.

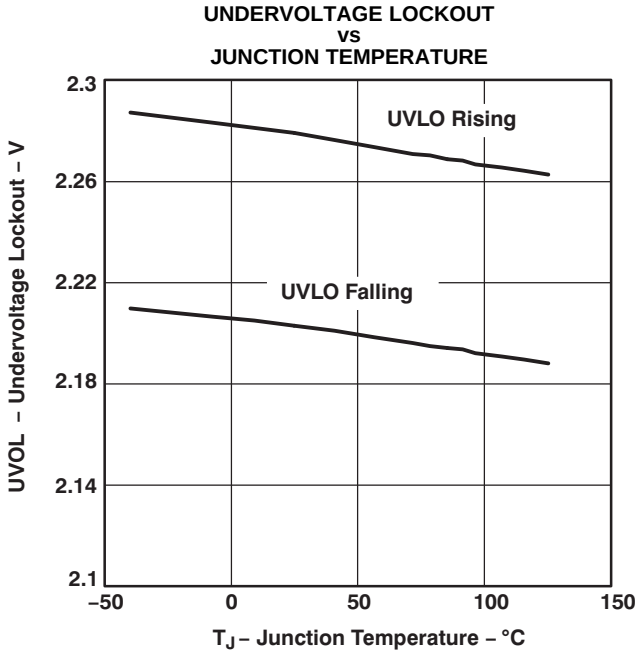


Figure 20.

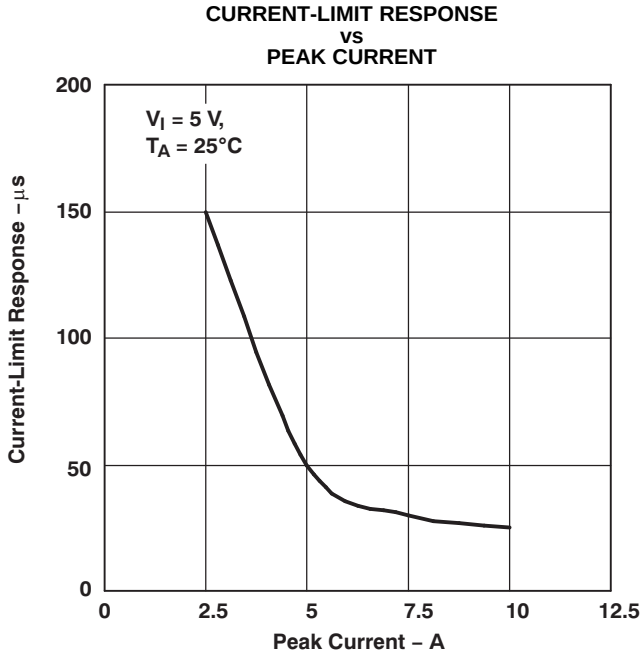


Figure 21.

APPLICATION INFORMATION

INPUT AND OUTPUT CAPACITANCE

Input and output capacitance improve the performance of the device; the actual capacitance should be optimized for the particular application. For all applications, a 0.01 µF to 0.1 µF ceramic bypass capacitor between IN and GND is recommended and should be placed as close to the device as possible for local noise de-coupling. This precaution reduces ringing on the input due to power-supply transients . Additional input capacitance may be needed on the input to reduce voltage overshoot from exceeding the absolute maximum voltage of the device during heavy transients.

Placing a high-value electrolytic capacitor on the output pin is recommended when the output load is heavy. Additionally, bypassing the output with a 0.01 µF to 0.1 µF ceramic capacitor improves the immunity of the device to short-circuit transients.

POWER DISSIPATION AND JUNCTION TEMPERATURE

The low on-resistance of the N-channel MOSFETs allows the small surface-mount packages to pass large currents. It is good design practice to check power dissipation to ensure that the junction temperature of the device is within the recommended operating conditions. The below analysis gives an approximation for calculating junction temperature based on the power dissipation in the package. However, it is important to note that thermal analysis is strongly dependent on additional system level factors. Such factors include air flow, board layout, copper thickness and surface area, and proximity to other devices dissipating power. Good thermal design practice must include all system level factors in addition to individual component analysis.

The following procedure shows how to approximate the junction temperature rise due to power dissipation in a single channel. The TPS2062A/66A devices contain two channels, so the total device power must sum the power in each power switch.

Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. Use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from the typical characteristics graph as an initial estimate. Power dissipation is calculated by:

$$P_D = r_{DS(on)} \times I_{OUT}^2$$

$$P_T = 2 \times P_D$$

Where:

P_D = Power dissipation/channel (W)

P_T = Total power dissipation for both channels (W)

$r_{DS(on)}$ = Power switch on-resistance (Ω)

I_{OUT} = Maximum current-limit threshold (A)

Finally, calculate the junction temperature:

$$T_J = P_T \times R_{\Theta JA} + T_A$$

Where:

T_A= Ambient temperature °C

$R_{\Theta JA}$ = Thermal resistance (°C/W)

P_T = Total power dissipation (W)

Compare the calculated junction temperature with the initial estimate. If they are not within a few degrees, repeat the calculation using the "refined" $r_{DS(on)}$ from the previous calculation as the new estimate. Two or three iterations are generally sufficient to achieve the desired result. The final junction temperature is highly dependent on thermal resistance $R_{\theta JA}$, and thermal resistance is highly dependent on the individual package and board layout. The "Dissipation Rating Table" at the begginng of this document provides example thermal resistances for specific packages and board layouts.

UNIVERSAL SERIAL BUS (USB) APPLICATIONS

One application for this device is for current-limiting in universal serial bus (USB) applications. The original USB interface was a 12-Mb/s or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (e.g., keyboards, printers, scanners, and mice). As the demand for more bandwidth increased, the USB 2.0 standard was introduced increasing the maximum data rate to 480-Mb/s. The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply. The USB specification classifies two different classes of devices depending on its maximum current draw. A device classified as low-power can draw up to 100 mA as defined by the standard. A device classified as high-power can draw up to 500 mA. It is important that the minimum current limit threshold of the current-limiting power switch exceed the maximum current limit draw of the intended application. The latest USB standard should always be referenced when considering the current-limit threshold.

The USB specification defines two types of devices as hubs and functions. A USB hub is a device that contains multiple ports for different USB devices to connect and can be self-powered (SPH) or bus-powered (BPH). A function is a USB device that is able to transmit or receive data or control information over the bus. A USB function can be embedded in a USB hub. A USB function can be one of three types included in the list below.

- Low-power, bus-powered function
- High-power, bus-powered function
- Self-powered function

SPHs and BPHs distribute data and power to downstream functions. The TPS206x6A has higher current capability than required for a single USB port allowing it to power multiple downstream ports.

SELF-POWERED AND BUS-POWERED HUBS

A SPH has a local power supply that powers embedded functions and downstream ports. This power supply must provide between 4.75 V to 5.25 V to downstream facing devices under full-load and no-load conditions. SPHs are required to have current-limit protection and must report overcurrent conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.

A BPH obtains all power from an upstream port and often contains an embedded function. It must power up with less than 100 mA. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This is accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than 100 mA. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

LOW-POWER BUS-POWERED AND HIGH-POWER BUS-POWERED FUNCTIONS

Both low-power and high-power bus-powered functions obtain all power from upstream ports. Low-power functions always draw less than 100 mA; high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 µF at power up, the device must implement inrush current limiting.

USB POWER-DISTRIBUTION REQUIREMENTS

USB can be implemented in several ways regardless of the type of USB device being developed. Several power-distribution features must be implemented.

- SPHs must:
  - Current-limit downstream ports
  - Report overcurrent conditions
- BPHs must:
  - Enable/disable power to downstream ports
  - Power up at <100 mA
  - Limit inrush current (<44 Ω and 10 μF)
- Functions must:
  - Limit inrush currents
  - Power up at <100 mA

The feature set of the TPS2062A/66A meets each of these requirements. The integrated current-limiting and overcurrent reporting is required by self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-powered hubs and the input ports for bus-powered functions.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TPS2062AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2062ADG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2062ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2062ADRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2062ADRBRG4	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2062ADRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2062ADRBTG4	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2062ADRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2066AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2066ADG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2066ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2066ADRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2066ADRBRG4	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2066ADRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2066ADRBTG4	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2066ADRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

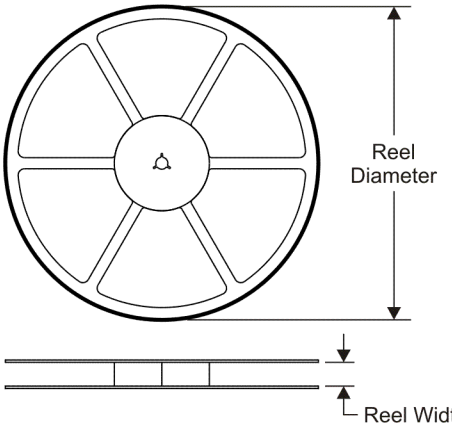
[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

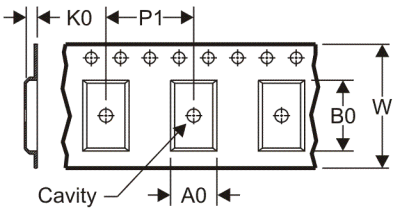
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

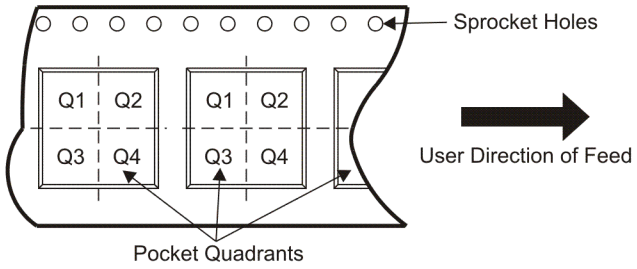


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

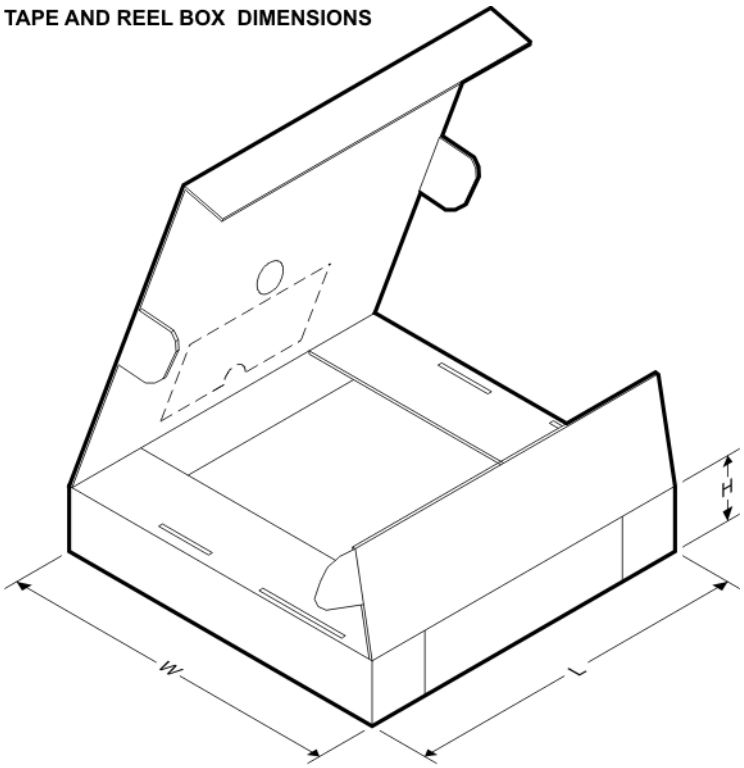
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2062ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2062ADRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS2062ADRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS2066ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2066ADRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS2066ADRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2

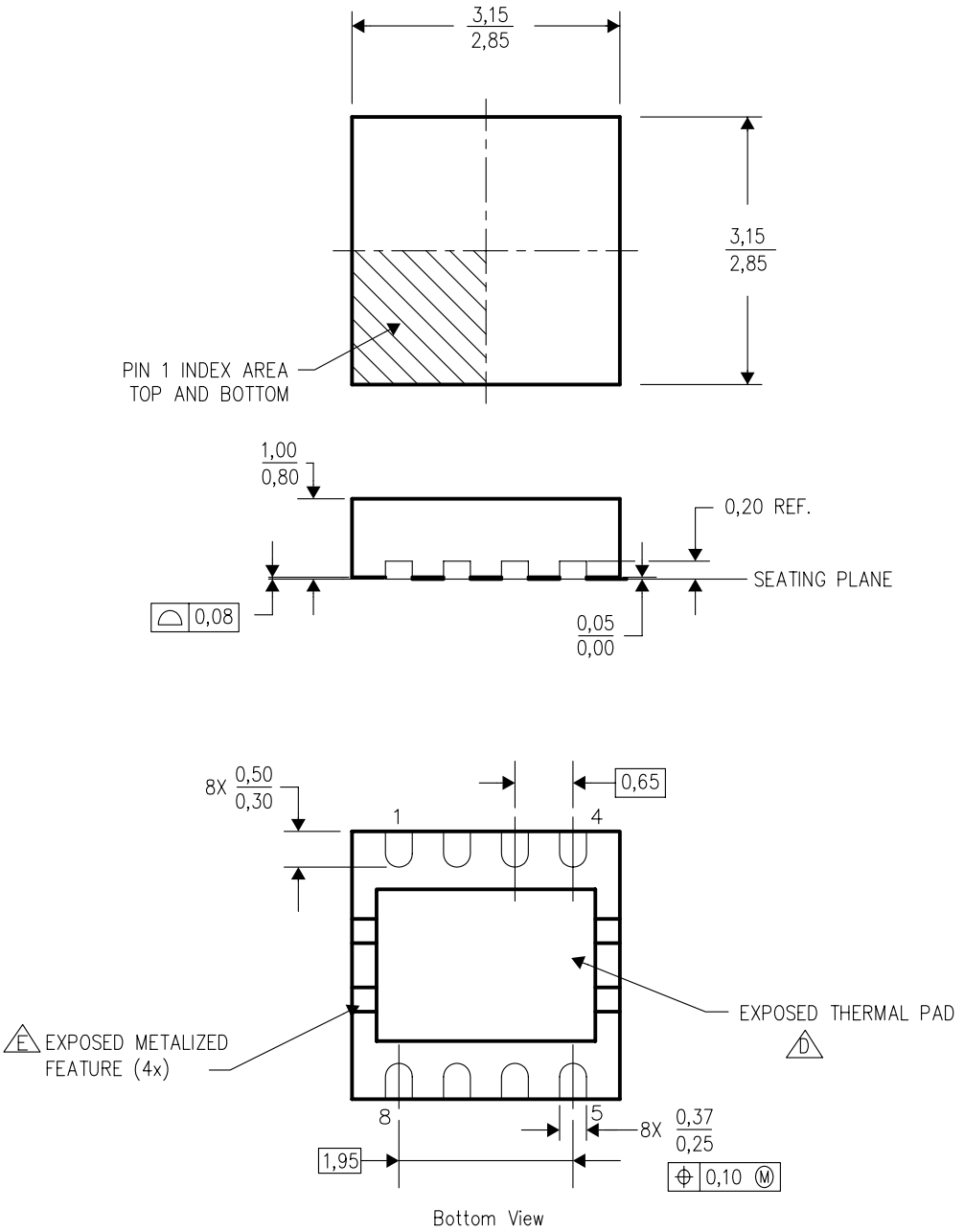
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2062ADR	SOIC	D	8	2500	340.5	338.1	20.6
TPS2062ADRBR	SON	DRB	8	3000	370.0	355.0	55.0
TPS2062ADRBT	SON	DRB	8	250	195.0	200.0	45.0
TPS2066ADR	SOIC	D	8	2500	340.5	338.1	20.6
TPS2066ADRBR	SON	DRB	8	3000	370.0	355.0	55.0
TPS2066ADRBT	SON	DRB	8	250	195.0	200.0	45.0

DRB (S–PDSO–N8) PLASTIC SMALL OUTLINE



4203482/G 11/04

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Metalized features are supplier options and may not be on the package.

THERMAL PAD MECHANICAL DATA

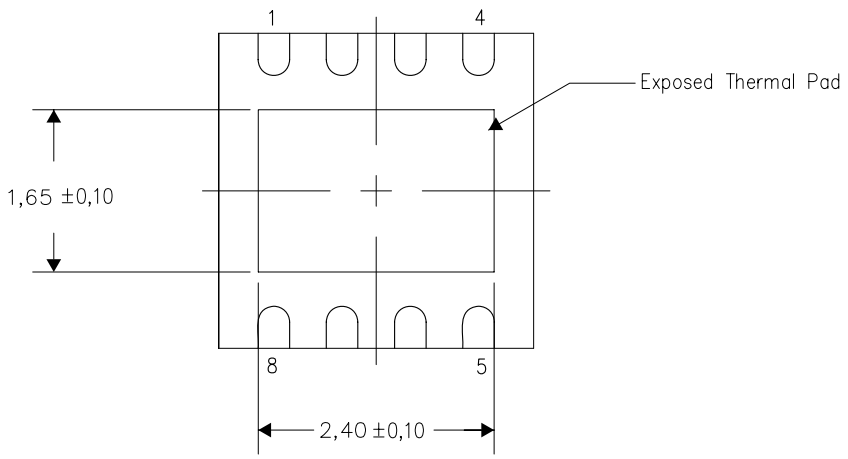
DRB (S–VSON–N8)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

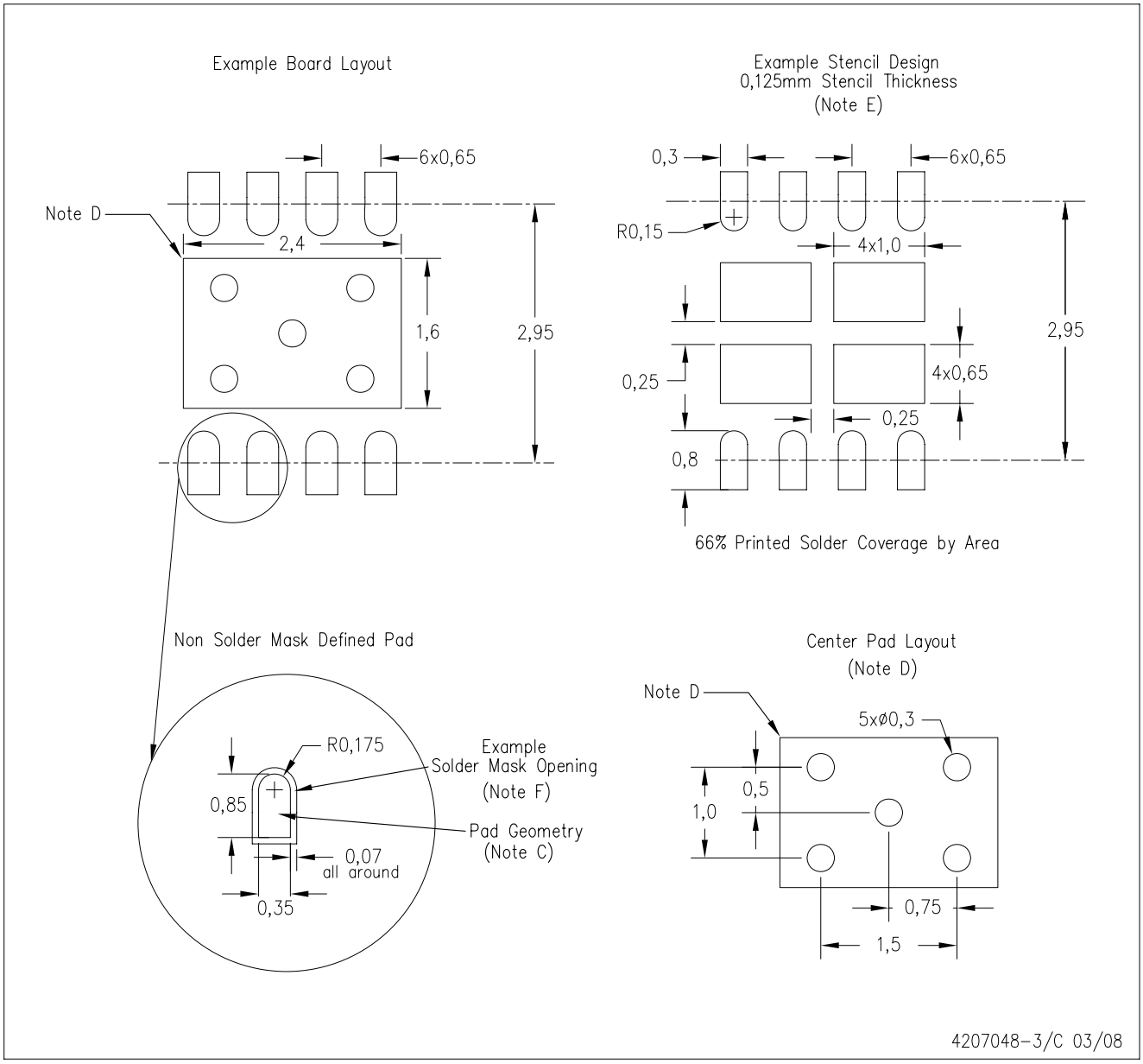


Bottom View

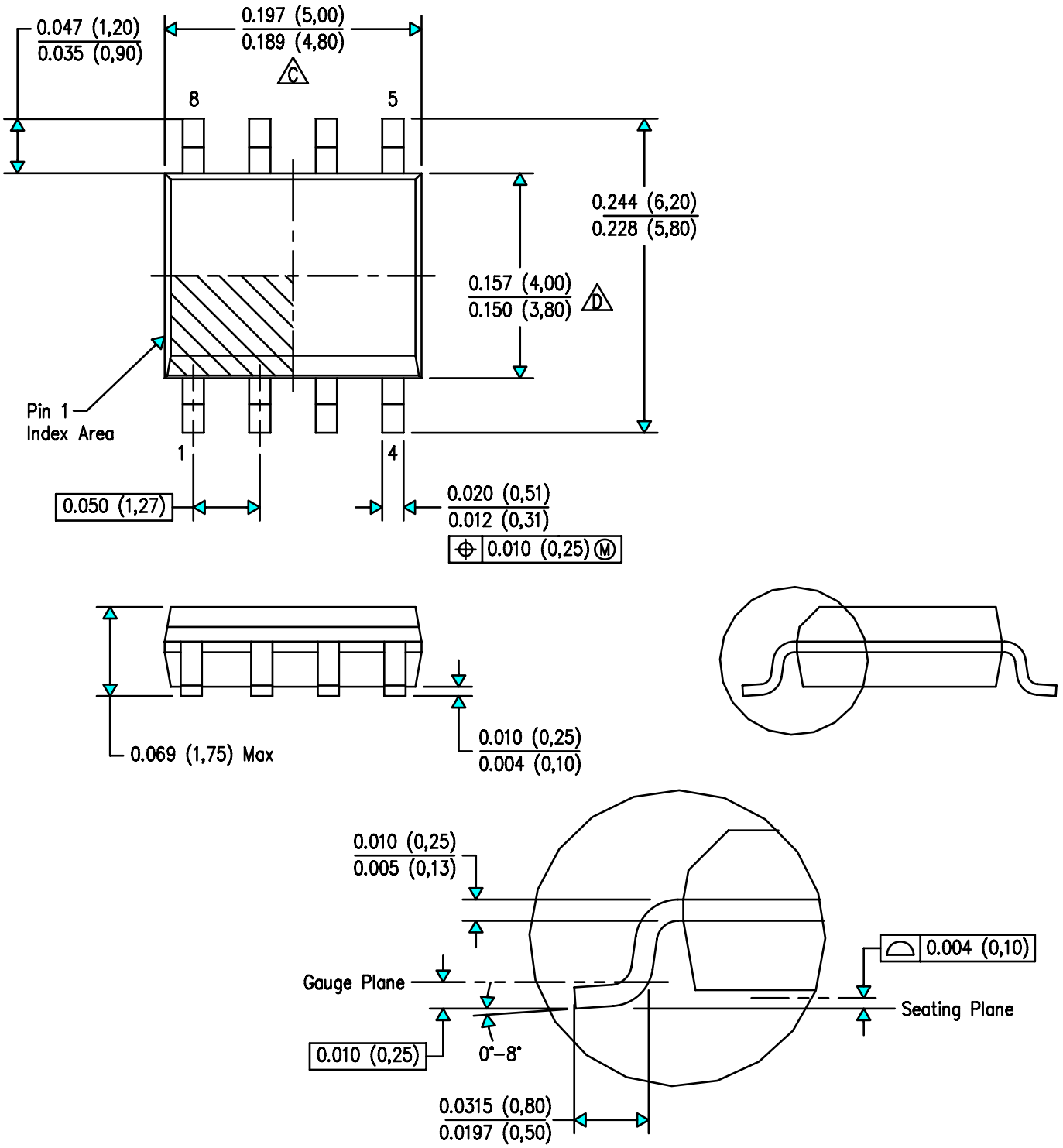
NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DRB (S–VSON–N8)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

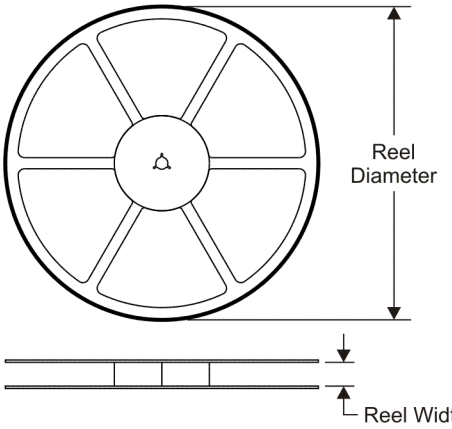


11/2008

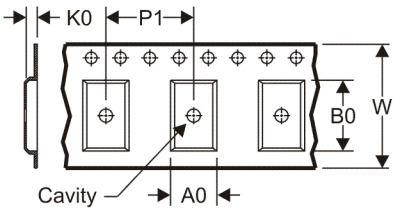
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



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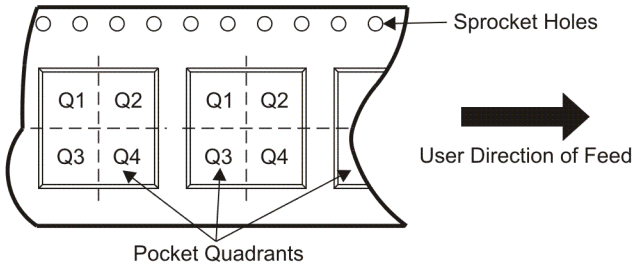
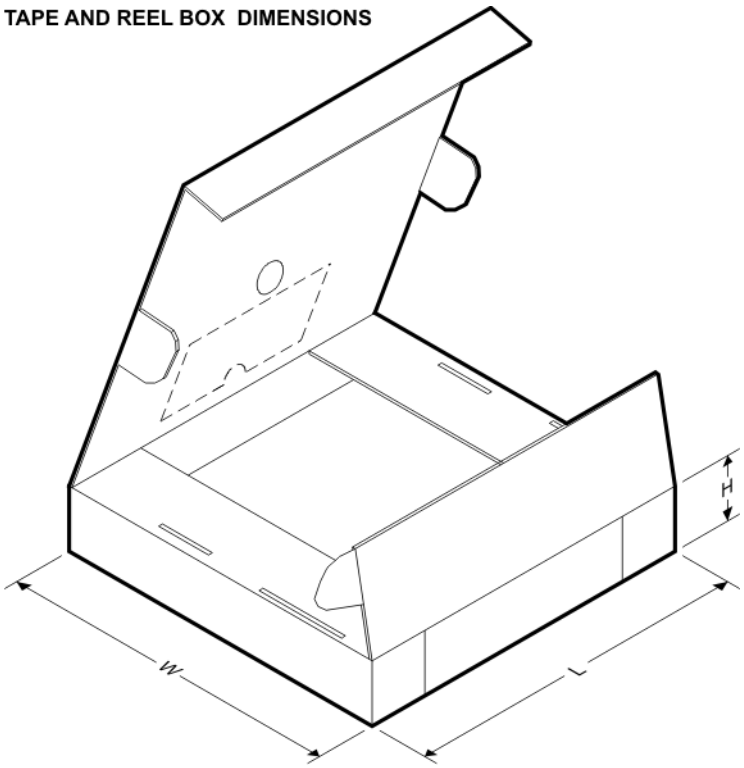
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2062ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2062ADRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS2062ADRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS2066ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2066ADRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS2066ADRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2062ADR	SOIC	D	8	2500	340.5	338.1	20.6
TPS2062ADRBR	SON	DRB	8	3000	370.0	355.0	55.0
TPS2062ADRBT	SON	DRB	8	250	195.0	200.0	45.0
TPS2066ADR	SOIC	D	8	2500	340.5	338.1	20.6
TPS2066ADRBR	SON	DRB	8	3000	370.0	355.0	55.0
TPS2066ADRBT	SON	DRB	8	250	195.0	200.0	45.0

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